capacitor storage is comprised of: a semiconductor layer extended from the first impurity region 217 and having a second impurity region (A) 219b, a second impurity region (B) 219c, and a region 218 that is not doped with any impurity element for setting the conductivity type of the region; an insulating layer of the same layer as a gate insulating film having a third shape; and a capacitor wiring line 225 that is formed form a conductive layer having a second taper shape.

In the light emitting device of this embodiment, if there is a pin hole in the EL layer 272, it causes a defect portion where the pixel electrode 271 and the cathode 273 are brought into contact through the pin hole. The defect portion can be changed into a transmuted portion 274 by the repairing method of the present invention, resulting in a raise in resistance. Therefore the other part of the pixel than the pin hole can have increased luminance and degradation of a part of the EL layer that surrounds the pin hole is not accelerated.

The structure of this embodiment can be combined with any of Embodiments 1, 2, 3, 4, 6, and 8.

[Embodiment 11]

An outline of a cross sectional structure of a light emitting display using the repair method of the present invention is explained in this embodiment.

Reference numeral 811 denotes a substrate in Fig. 18, and reference numeral 812 denotes an insulating film which becomes a base (hereafter referred to as a base film). A light transmitting substrate, typically a glass substrate, a quartz substrate, a glass ceramic substrate, or a crystalline glass substrate can be used as the substrate 811. However, the substrate used must be one able to withstand the highest process temperature during the manufacturing processes.

Further, the base film 812 is particularly effective when using a substrate containing mobile ions or a substrate which has conductivity, but the base film 812 need not be formed on a quartz substrate. An insulating film containing silicon may be used as the base film 812. Note that the term insulating film containing silicon specifically indicates an insulating film such as a silicon oxide film, a silicon nitride film, and a silicon oxynitride film (denoted as SiOxNy, where x and y are arbitrary integers) containing oxygen or nitrogen at predetermined ratios with respect to silicon.

Reference numeral 8201 denotes a switching TFT, reference numeral 8202 denotes an EL driver TFT, and both are formed by n-channel TFT and p-channel TFTs respectively. When the direction of EL light emitted is toward the substrate lower side (surface where TFTs and the EL layer are not formed), the above structure is preferable. However, the present invention is not limited to this structure. The switching TFT and the EL driver TFT may be either n-channel TFTs or p-channel TFTs.

The switching TFT 8201 has an active layer containing a source region 813, a drain region 814, LDD regions 815a to 815d, a separation region 816, and an active layer including channel forming regions 863 and 864, a gate insulating film 818, gate electrodes 819a and 819b, a first interlayer insulating film 820, a source signal line 821 and a drain wiring 822. Note that the gate insulating film 818 and the first interlayer insulating film 820 may be common among all TFTs on the substrate, or may differ depending upon the circuit or the element. In addition, the reference numeral 817a and 817b are masks to form the channel forming region.

Furthermore, the switching TFT 8201 shown in Fig. 18 is electrically connected to the gate electrodes 819a and 819b, becoming namely a double gate structure. Not only the double gate structure, but also a multi-gate structure (a structure containing an active

layer having two or more channel forming regions connected in series) such as a triple gate structure, may of course also be used.

The multi-gate structure is extremely effective in reducing the off current, and provided that the off current of the switching TFT is sufficiently lowered, a capacitor connected to the gate electrode of the first EL driver TFT 8202 can be have its capacitance reduced to the minimum necessary. Namely, the surface area of the capacitor can be made smaller, and therefore using the multi-gate structure is also effective in expanding the effective light emitting surface area of the EL elements.

In addition, the LDD regions 815a to 815d are formed so as not to overlap the gate electrodes 819a and 819b through the gate insulating film 818 in the switching TFT 8201. This type of structure is extremely effective in reducing the off current. Furthermore, the length (width) of the LDD regions 815a to 815d may be set from 0.5 to 3.5 μm, typically between 2.0 and 2.5 μm.

Note that forming an offset region (a region which is a semiconductor layer having the same composition as the channel forming region and to which the gate voltage is not applied) between the channel forming region and the LDD region is additionally preferable in that the off current is lowered. Further, when using a multi-gate structure having two or more gate electrodes, the separation region 816 (a region to which the same impurity element, at the same concentration, as that added to the source region or the drain region, is added) is effective in reducing the off current.

Next, the first EL driver TFT 8202 is formed having an active layer containing a source region 826, a drain region 827, and a channel forming region 805; the gate insulating film 818; a gate electrode 830, the first interlayer insulating film 820; a source wiring 831; and a drain wiring 832. The first EL driver TFT 8202 is a p-channel TFT in Embodiment 11. The reference numeral 829 is a mask to form the channel forming region.